WHAT IS CLAIMED IS:

1. A logic circuit comprising:

a dynamic logic portion for evaluating a Boolean function of a plurality of data input signals, wherein a logic signal on a dynamic node asserted in response to a first logic state of a clock signal comprises either a logic true or a logic false Boolean combination of the plurality of the data input signals and the dynamic node is pre-charged to a first logic state corresponding to the logic false Boolean combination when the clock signal has a second logic state;

a static portion having a pull-down input, a data input coupled to the dynamic node, a data output node generating a latched data output signal in response to the logic signal and the clock signal, and an inverted data output node generating a latched inverted data output signal as the logic inversion of the latched data output signal, wherein the inverted data output node is set to a logic zero when the pull-down input is a logic one and the inverted data output node is held at a logic zero when the data output signal is a logic one; and

a feedforward pulse circuit having a first input coupled to the dynamic node, a second input coupled to the inverted data output node, and a pulse node coupled to the pull-down input and generating a feedforward pulse, wherein the feedforward pulse is a logic one when the dynamic node is a logic zero and the inverted data output signal is a logic one.

2. The logic circuit of claim 1, wherein the dynamic logic portion comprises:

a first P channel field effect transistor (PFET) having a gate terminal coupled to the clock signal, a source terminal coupled to a positive power supply voltage and a drain terminal coupled to the dynamic node, wherein the dynamic node is coupled to the positive power supply voltage in response to the first logic state of the clock signal and isolated from the positive power supply voltage in response to a second logic state of the clock signal;

a logic tree having a plurality of logic inputs, a positive tree terminal coupled to the dynamic node, and a negative tree terminal, wherein the positive tree terminal is coupled to the negative tree terminal in response to first logic states of the plurality of logic inputs and isolated from the negative tree terminal in response to second logic states of the plurality of logic inputs; and

a first N channel FET (NFET) having a gate terminal coupled to the clock signal, a drain terminal coupled to the negative tree terminal and a source terminal coupled to a negative power supply voltage, wherein the negative tree terminal is coupled to the negative power supply voltage in response to the second logic state of the clock signal and isolated from the negative power supply voltage in response to a first logic state of the clock signal.

3. The logic of claim 1 wherein the static portion comprises:

a first PFET having a gate coupled to the dynamic node, a source coupled to the first power supply voltage and a drain;

a first NFET having a gate coupled to the gate of the first PFET, a drain coupled to the drain of the first PFET for a data output node generating the data output signal, and a source;

a second NFET having a gate coupled to the second clock signal, a source coupled to the second power supply voltage and a drain coupled to the source of the first NFET;

a third NFET having a drain coupled to the drain of the second NFET, a source coupled to the second power supply voltage and a gate;

an inverting circuit having an input coupled to the data output node and an output coupled to the inverted data output node;

a fourth NFET having a source coupled to the second power supply voltage, a drain coupled to the inverted data output node, and a gate coupled to the pull-down input; and

and a second PFET having a gate coupled to the output node of the inverting circuit, a drain coupled to the data output node and a source coupled to the first power supply voltage.

4. The logic circuit of claim 1, wherein the feedforward pulse circuit comprises:

a first NFET having a source coupled to the second power supply voltage, a drain and a gate coupled to the dynamic node;

a first PFET having a drain coupled to the drain of the first NFET forming the pulse node, a gate coupled to the dynamic node and a source;

a second PFET having a drain coupled to the source of the first PFET, a source coupled to the first power supply voltage and a gate; and

an inverter having an input coupled to the inverted data output node, and output coupled to the gate of the first PFET.

5. The logic circuit of claim 3, wherein the inverting circuit comprises:

a third PFET having a gate coupled to the data output node, a source coupled to the first power supply voltage and a drain; and

a fifth NFET having a gate coupled to the gate of the third PFET, a source coupled to the second power supply voltage and a drain coupled to the drain of the third PFET forming the inverted data output node.

6. The logic circuit of claim 5, wherein the fourth NFET is substantially larger than the fifth NFET.

7. The logic circuit of claim 6, wherein the fourth NFET is about ten times larger than the fifth NFET.

8. The logic circuit of claim 6, wherein all PFETs and all NFETs in a logic path driving the fifth NFET may be made smaller when the fourth NFET is made substantially larger than the fifth NFET.

9. A data processing system comprising:

a central processing unit (CPU); and

a memory operable for communicating instructions and operand data to the CPU which includes a logic system having a logic circuit with a dynamic logic portion for evaluating a Boolean function of a plurality of data input signals, wherein a logic signal on a dynamic node asserted in response to a first logic state of a clock signal comprises either a logic true or a logic false Boolean combination of the plurality of the data input signals and the dynamic node is pre-charged to a first logic state corresponding to the logic false Boolean combination when the clock signal has a second logic state, a static portion having a pull-down input, a data input coupled to the dynamic node, a data output node generating a latched data output signal in response to the logic signal and the clock signal, and an inverted data output node generating a latched inverted data output signal as the logic inversion of the latched data output signal, wherein the inverted data output node is set to a logic zero when the pull-down input is a logic one and the inverted data output node is held low when the data output signal is a logic one; and a feedforward pulse circuit having a first input coupled to the dynamic node, a second input coupled to the inverted data output node, and a pulse node coupled to the pull-down input and generating a feedforward pulse, wherein the feedforward pulse is a logic one when the dynamic node is a logic zero and the inverted data output signal is a logic one.

10. The data processing system of claim 9, wherein the dynamic logic portion comprises:

a first P channel field effect transistor (PFET) having a gate terminal coupled to the clock signal, a source terminal coupled to a positive power supply voltage and a drain terminal coupled to the dynamic node, wherein the dynamic node is coupled to the positive power supply voltage in response to the first logic state of the clock signal and isolated from the positive power supply voltage in response to a second logic state of the clock signal;

a logic tree having a plurality of logic inputs, a positive tree terminal coupled to the dynamic node, and a negative tree terminal, wherein the positive tree terminal is coupled to the negative tree terminal in response to first logic states of the plurality of logic inputs and isolated from the negative tree terminal in response to second logic states of the plurality of logic inputs; and

a first N channel FET (NFET) having a gate terminal coupled to the clock signal, a drain terminal coupled to the negative tree terminal and a source terminal coupled to a negative power supply voltage, wherein the negative tree terminal is coupled to the negative power supply voltage in response to the second logic state of the clock signal and isolated from the negative power supply voltage in response to a first logic state of the clock signal.

11. The data processing system of claim 9 wherein the static portion comprises:

a first PFET having a gate coupled to the dynamic node, a source coupled to the first power supply voltage and a drain;

a first NFET having a gate coupled to the gate of the first PFET, a drain coupled to the drain of the first PFET for a data output node generating the data output signal, and a source;

a second NFET having a gate coupled to the second clock signal, a source coupled to the second power supply voltage and a drain coupled to the source of the first NFET;

a third NFET having a drain coupled to the drain of the second NFET, a source coupled to the second power supply voltage and a gate;

an inverting circuit having an input coupled to the data output node and an output coupled to the inverted data output node;

a fourth NFET having a source coupled to the second power supply voltage, a drain coupled to the inverted data output node, and a gate coupled to the pull-down input; and

and a second PFET having a gate coupled to the output node of the inverting circuit, a drain coupled to the data output node and a source coupled to the first power supply voltage.

12. The data processing system of claim 9, wherein the feedforward pulse circuit comprises:

a first NFET having a source coupled to the second power supply voltage, a drain and a gate coupled to the dynamic node;

a first PFET having a drain coupled to the drain of the first NFET forming the pulse node, a gate coupled to the dynamic node and a source;

a second PFET having a drain coupled to the source of the first PFET, a source coupled to the first power supply voltage and a gate; and

an inverter having an input coupled to the inverted data output node, and output coupled to the gate of the first PFET.

13. The data processing system of claim 11, wherein the inverting circuit comprises:

a third PFET having a gate coupled to the data output node, a source coupled to the first power supply voltage and a drain; and

a fifth NFET having a gate coupled to the gate of the third PFET, a source coupled to the second power supply voltage and a drain coupled to the drain of the third PFET forming the inverted data output node.

14. The data processing system of claim 13, wherein the fourth NFET is substantially larger than the fifth NFET.

15. The data processing system of claim 14, wherein the fourth NFET is about ten times larger than the fifth NFET.

16. The logic circuit of claim 14, wherein all PFETs and all NFETs in a logic path driving the fifth NFET may be made smaller when the fourth NFET is made substantially larger than the fifth NFET.